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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)		
	)		
Venkitakrishnan et al.	)	Examiner:	Knoll, C. H.
	)		
Serial No.: 09/916,598	)	Art Unit:	2112
	)		
Filing Date: July 26, 2001	)		
	)		
For: A CACHE COHERENT SPLIT TRANSACTION MEMORY BUS ARCHITECTURE AND PROTOCOL FOR A MULTI PROCESSOR CHIP DEVICE	)		

RESPONSE TO OFFICE ACTION

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed January 7, 2003, Applicants respectfully request reconsideration of the above referenced patent application. Please consider the following remarks for allowance of the above identified patent application.